REMARKS

Applicants respectfully traverse and request reconsideration.

In the Drawings, Figure 1 is now designated as Prior Art to clarify that which is old. Furthermore, typographical and cosmetic errors have been corrected in Figure 4. These changes are shown marked in red on a separate page, while another page shows the corrections made in black.

In addition, the headings of the Specification have been changed to uppercase although the guidelines established in 37 CFR 1.77(b) are not mandatory.

Lastly the Applicants have correct a typographical error in the Specification on page 10 in order to clarify any possible misunderstandings.

Claims 1-3, 6-8, 21-23 and 26-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,052,129 ("Fowler").

The Koss reference is directed to a computer graphics system having high performance primitive clipping preprocessing. Specifically, Koss teaches a clipping preprocessor circuit able to perform an evaluation of a relationship between primitive vertex data from the vertex input data path and a clip region, and to provide a signal on the control output based on this evaluation (Col. 2, Lines 17-21). The computer graphics system includes a front end board, a texture mapping board, and a frame buffer board (Col. 4, Lines 32-34; Figure 1). The front end board is of primary interest as it includes a plurality of 3-D geometry accelerator chips that, inter alia, contain the clipping preprocessing circuitry or clip code logic unit (Col. 8, Lines 15-19). The clipping preprocessor can include X, Y and Z coordinate preprocessing circuitry, which can each include memory cells in a shift register and combinational logic circuitry operatively connected to outputs of the memory cells (Col. 2, Lines 30-34). Figure 4 is a block diagram of an X coordinate clipping preprocessing circuit that forms part of the geometry accelerator. The clipping preprocessing circuit includes a maximum clipping extent register, a clipping vertex coordinate register, and a minimum clipping extent register.

The maximum and minimum clipping extent registers define the boundaries of a clip region while the clipping vertex coordinate register contains the vertex coordinate value (X, Y or Z) for a specific vertex of a polygon primitive. Two floating point comparators (Figure 4, Elements 206 and 208) are connected to the outputs of the three registers such that a comparison can be made between the maximum clipping extent register value and the clipping vertex coordinate register value and between the minimum clipping extent register value and the clipping vertex coordinate register value. Each of the floating point comparators compares the two floating point numbers it receives and provides a signal that indicates which one is larger (Col. 8, Lines 42-44).

The first comparator generates a maximum flag bit while the second comparator generates a minimum flag bit. Together this pair of flag bits is termed a "clip subcode" and is loaded in a shift register (Col. 11 Line 67 – Col. 12, Line 10). The process continues for a single vertex such that a clip code word is generated. One clip code word contains three clip subcodes for each of the three dimensions (X, Y or Z). The process continues until a clip code is generated for each vertex within a polygon and stored in respective shift registers (Figure 4, Elements 220, 224, 246, & 248). Once clip code words are generated, a trivial accept or trivial reject signal is produced and output from the preprocessing circuit to a handshaking control unit (Figure 1, Element 107). If the primitive is not trivially accepted or rejected, the clip code words stored in the registers are transferred to the right stack control unit (Figure 1, Element 152). If the primitive is trivially accepted or rejected, the clip code word is not transferred (Col. 12, Lines 22-33).

The trivial accept signal is produced if all vertices of a polygon have X, Y and Z coordinates between the minimum X, Y and Z extent values and the maximum X, Y and Z extent values. This corresponds to all vertices, and therefore the entire primitive, falling within the clip region. (Col. 13, Lines 53-61). The handshaking control unit (Figure 1, Element 107) responds to the trivial accept signal by sending a trivial accept flag to the right stack control unit (Figure 1, Element 152) disabling any clipping on this primitive before display.

The trivial reject signal is produced if all vertices of the primitive are found in one of six half spaces outside of the clip region. These half spaces include the space in which the X, Y and Z coordinates are either above the maximum extent value or below the minimum extent value. (Col. 13, Lines 62 – Col. 14, Line 3).

In some cases, neither a trivial accept or a trivial reject signal is asserted and the clipping processor performs clipping operations on the primitive. In many cases this may still result in the primitive not being displaced, since the clip code logic unit (or clipping preprocessor) does not trivially reject all rejectable primitives (Col. 13, Lines 44-52). This is demonstrated in Figure 11 of Koss.

Lastly, the method of Koss may include a case in which display parameters are generated for a primitive when the preprocessor fails to determine that all of the primitive coordinates lie outside the clip region (Col. 2, Line 64 – Col. 3, Line 2).

The Fowler reference is directed to a separate method and apparatus for deferred clipping of polygons. Exploiting the tendency of most polygons to be wholly inside of or wholly outside of the view volume (frustum), Fowler teaches a method of clipping in which most of the clipping steps are removed from the commonly executed graphics pipeline. The rasterization step is augmented whereby the rasterizer utilizes guardband regions about the clip volume, such that polygons requiring clipping (i.e., those that cannot be trivially accepted by the view volume and cannot be trivially accepted by the guardband region) occur only in rare circumstances. While executing the standard graphics processing steps, problem polygons (i.e., those outside of the guardband) are buffered for later processing, while the standard graphics processing continues without the need for periodically reformatting data and performing clipping (Col. 3, Lines 31-54). A guardband region, such as illustrated in Figure 9 or Fowler is provided at the periphery of a 3-D region, representing the clip volume. The guardbands are introduced as a way to reduce the number of clipping operations and to increase the number of trivial accepts and rejects. All objects falling entirely inside of the guardband regions are trivially accepted. Objects that are entirely outside of at least one boundary of the clip region are

trivially rejected. All other objects will require clipping against the clip region, and are sent by the rasterizer to a buffer for later clip processing (Col. 6, 7-21).

With respect to Claim 1, the Applicants respectfully believe that no combination of the Koss reference or the Fowler reference discloses the Applicants' claimed invention. The Applicants agree with the Office Action that admits Koss does not teach, inter alia, a discard clip guard bands for clipping processing. The Office Action cites Koss in view of Fowler as disclosing a method of comparing at least one vertex with X, Y and Z clip values to determine an X, Y and Z clip code where the X, Y and Z clip values correspond to the minimum and maximum X, Y and Z values for the display space scaled to include a discard clip guard band (horizontal or vertical). However, while Koss teaches a method of comparing a vertex coordinate value to a minimum and maximum extent value of the display screen, Koss fails to teach clip values scaled to include a discard clip guard band as claimed by Applicants.

Furthermore, Fowler also fails to teach a discard clip guard band. Fowler discloses a guardband that is inherently different from a horizontal or vertical discard clip guard band. The guardband of Fowler is referenced by Applicants as a trivial accept guard band (Figure 1 of Specification) and is considered known in the art to reduce the number of clipping operations that must be performed on primitives in order to generate the displayed image (Pg. 4, Line 29 – Pg. 5, Line 2). The Applicants' claimed invention relies upon a non-obvious trivial discard guard band (Figure 2, Element 30), constructed from the horizontal and vertical discard clip guard bands, that expands the display screen minimum and maximum coordinate values. The claimed trivial discard guard band allows the discarding of primitives that would otherwise be processed using only a trivial acceptance band as taught by Fowler.

In prior art systems line primitive 40 and point primitive 50 of Applicants' Figure 2, whose rasterization area is part of the display area, would often be discarded because their vertices lie outside of the display screen. Koss teaches a system that would trivially discard these two primitives based upon the location of their vertices with respect to the display area. Without a trivial discard guard band, Koss's system would realize

unwanted display aberrations (Pg. 6, Lines 14-18). In the Applicants' claimed invention, if the trivial accept guard band was properly sized, both primitives would be properly processed rather than being discarded thereby avoiding the discarding of primitives that contribute to the image data of the frame. The Applicants' claimed method would entail the trivial discard guard band first not rejecting the primitive, and then the trivial accept guard band making an accept decision.

Fowler teaches a method in which line primitive 40 and point primitive 50 (Applicants' Figure 2) would be processed. However, Fowler's system would also process line primitive 60 (Applicants' Figure 2) which contributes no pixel information to the display area and therefore limit system efficiency. The Applicants' claimed invention would discard line primitive 60 because of the X, Y and Z clip code values determined when comparing each vertex to the discard guard band values.

The Applicants respectfully believe that Claim 1 is allowable as any combination of prior art fails to disclose the Applicants' claimed invention. Moreover the motivation to combine Koss and Fowler, as cited by the Office Action, is moot under the pretense that the combination of Koss and Fowler teaches a one guard band clipping system utilizing a high performance comparison circuit. In essence, Koss and Fowler teach a high performance version of prior art as stated in the Applicants' Background of the Invention, while it is inherent that the Applicants' claimed invention relies upon both a discard and accept guard band. The Applicants' specification serves as the only source for a motivation to combine Koss and Fowler, and is therefore invalid.

With respect to Claim 2, the Applicants respectfully restate the relevant remarks from the response to Claim 1 while also adding that Claim 2 is dependant upon an allowable base claim and contains further patentable material. Applicants believe Claim 2 to be allowable.

In regards to Claim 3, the Applicants respectfully restate the relevant remarks made from the response to Claim 1. Specifically, the Applicants note that Fowler does not teach a trivial discard guard band, and therefore does not teach its constituent members, the horizontal or vertical discard clip guard bands. In one embodiment, the

horizontal and vertical discard clip guard bands correspond to scaled minimum and maximum coordinate values of the display screen, while in other embodiments they can be based on a dimension of a rasterized area of a particular primitive. For example, the primitive may be a line primitive, and the trivial discard guard band is sized to ensure that the width of the line, which is the smaller dimension of the rasterized area of the line, is taken into account when trivial discard determinations are made. By sizing the trivial discard guard band to correspond to a rasterized area, the line will continue to contribute some pixel information to the display until the point where all of the rasterized area of the line lies external to the display space (Page 9, Lines 14-26). This aspect of the Applicants' claimed invention is neither taught nor made obvious by any combination of Fowler and Koss. Furthermore, the Office Action cites Fowler Column 6, Lines 7-20 as disclosing discard clip guard bands based on a dimension of a rasterized area of the primitive (triangle). However, this reference merely discussed the use of Fowler's guardbands, different from Applicants' claimed trivial discard guard band, as a way to reduce the number of clipping operations and to increase the number of trivial accepts and rejects. Fowler does not teach or make obvious the Applicants' claimed invention to one of ordinary skill in the art at the time of the invention. In addition, Claim 3 is dependent upon an allowable base claim. The Applicants' believe Claim 3 to be allowable.

With respect to Claim 6, the Applicants respectfully restate the relevant remarks from the response to Claims 1 and 3. The Office Action incorrectly cites Column 8, Lines 20-23 of Fowler as disclosing horizontal and vertical discard clip guard bands corresponding to an amount of dimensional expansion used for processing primitives. Furthermore, the Office Action relates the horizontal discard clip guard band to a z coordinate, the vertical discard clip guard band to a Y coordinate, and the dimensional expansion to an infinitely large guard band W value. The Applicants respectfully believe Fowler to teach the process of transforming perspective coordinates (X, Y, Z and W) into normalized device coordinates by dividing the Z, Y and Z coordinates by the W coordinate which carries the perspective information necessary to represent a perspective transformation. The cited reference of Column 8, Lines 20-23 discusses a specific case in which the quantity (Z/W) may get infinitely large and therefore not allowing the system

to provide accurate normalized device coordinates to the rasterizer for the pre-clipping clip code computation step. As a result, the Applicants respectfully believe that Fowler fails to teach or make obvious the Applicants' claimed invention. In addition, Claim 6 is dependent upon Claim 3, an allowable base claim. The Applicants respectfully believe Claim 6 to be allowable.

As to Claim 7, the Applicants respectfully restate the relevant remarks from the response to Claims 1 and 6. Claim 7 discloses dimensional expansion corresponding to anti-aliasing operations performed on primitives having at least three vertices. The Office Action cites Fowler (Col. 6, Line 28) as teaching this additional patentable material. However, this reference merely states that anti-aliasing can be performed by a rasterizer when the rasterizer has certain state information that affects how triangles are rendered. This is not analogous to the Applicants' claimed invention in which the horizontal and vertical discard clip guard bands are sized to correspond to dimensional expansion relating to anti-aliasing operations. As a result of this knowledge and the dependency of Claim 7 on allowable Claim 6, the Applicants respectfully believe Claim 7 to be allowable.

In regards to Claim 8, the Applicants restate the relevant remarks from the response to Claim 1. The Office Action cites Fowler (Col. 8, Lines 20-26) as disclosing horizontal and vertical clip guard bands corresponding to dimensions corresponding to a predetermined number of pixels. This reference was also used for Claim 6, and the relevant remarks from the response to Claim 6 also apply to Claim 8. The pre-clipping clip code computation step of Fowler is not analogous to the claim language of Applicants' Claim 8 in which a determined size of the trivial discard guard band may be found acceptable. In such a system, premature discarding of line primitives may occur, but the resulting effect would also be minimal (Page 10, Lines 11-18). Fowler's pre-clipping code computation step refers to process in which clip codes are generated or computed for the clip testing process (Col. 2, Lines 13-23).

With respect to Claim 21, the Applicants respectfully restate the relevant remarks for Claim 1 as Claim 21 corresponds to a primitive processor comprising a processing

module and operating instructions stored in memory able to perform the methods described in Claim 1. As such the Applicants respectfully believe Claim 21 to be allowable.

Claims 22, 23 and 26-28 correspond to the primitive processor able to execute the methods described in Claims 2, 3 and 6-8, respectively, and are therefore believed to be allowable per the relevant remarks made above.

Claims 4, 5, 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,052,129 ("Fowler") and further in view of U.S. Patent No. 5,012,433 ("Callahan").

Callahan is directed to a multistage clipping method for clipping two and three dimensional graphic primitives for use in a computer graphics workstation. During the first clipping stage, the system removes all graphic primitives which lie outside of an arbitrary clipping volume or window. This arbitrary clipping volume or window is an enlargement of the desired viewing window, and the clipped image is projected and mapped onto a virtual viewport, also larger than the real viewport. Upon completion or this mapping, rendering effects are applied and finally the last stage of clipping is applied in which the virtual viewport is clipped to the real viewport (the final display area). This process allows rendering effects to be more correctly carried out (See Abstract; Figure 7).

With respect to Claim 4, the Office Action cites Callahan as disclosing the language of Claim 4 in which the Applicants' method of Claim 1 relies upon horizontal and vertical discard clip guard bands based on one-half of a smaller dimension of the rasterized area of a line primitive. The Applicants respectfully restate the relevant remarks made in response to Claims 1 and 3, and furthermore notes that Column 7, Lines 8-25 of Callahan do not disclose the Applicants' claimed invention. Rather, this reference is specifically directed to the process of the first clipping stage described above in which the system removes all graphic primitives which lie outside of an arbitrary clipping volume or window (often larger than the desired clipping volume). Callahan is silent as to trivial discard guard bands and their constituent members, the horizontal and vertical discard clip guard bands. Furthermore, Callahan is silent as to basing the

horizontal and vertical discard clip guard bands upon one half of a smaller dimension of the rasterized area of the line. As a result, Callahan does not make obvious the Applicants' claimed invention, and the Applicants respectfully believe that Claim 4 is allowable as it contains further non-obvious patentable material.

In regard to Claim 5, the Applicants claim the method of Claim 1 and 3 in which the horizontal and vertical discard clip bands are based on a radial dimension of the rasterized area of a point primitive. This is not analogous to Koss in view of Callahan. Koss does disclose clipping preprocessing for various polygon primitives (triangle, line, and point), but is silent as to any type of discard clip bands. Furthermore, while Callahan teaches a method of clipping inclusive of the rasterized area of a point primitive, Callahan is also silent on discard clip bands. The Applicants restate the relevant remarks in response to Claims 1, 3, and 4, and believe Claim 5 is allowable as it contains further non-obvious patentable material.

Claims 24 and 25 are in reference to the primitive processor able to execute instructions stored in memory corresponding to the functions described in Claims 4 and 5. As Claims 4 and 5 are allowable, Claims 24 and 25 are also believed to be allowable.

Claims 9, 10, 29 and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over four different references namely, U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,052,129 ("Fowler") and further in view of U.S. Patent No. 5,369,741 (Hartog) and U.S. Patent No. 6,359,630 (Morse).

Hartog is directed to a method for pre-clipping a line lying within a clipping rectangular region which is a subset of a region of a display screen. A method is provided for pre-clipping lines based on the relationship of the endpoints of the lines to both the specified rectangular clipping area, and the typically larger graphic device coordinate space (Col. 2, Lines 45-49). Upon determining the specified areas (the clipping area and the graphic device coordinate space), the system generates outcodes defining the endpoints of the line and then prepares a logical decision whether or not to draw the said line. A decision is made not to draw the line in the event both endpoints of the line fall outside the specified clipping area, to draw the line in the event one endpoint

of the line falls within the specified clipping area and the other endpoint falls inside the larger area, or to not draw the line in the event at least one endpoint falls outside the larger area (Col. 4, Lines 13-29).

With respect to Claim 9, the Applicants respectfully restate the relevant remarks made in response to Claim 1 with respect to the Koss reference; accordingly this claim is allowable. In addition, their combination with Hartog and Morse fails to disclose the Applicants' claimed invention. Hartog relies upon two sets of generated outcodes describing the location of a line segment via its endpoints. A scissor clipper (Figure 3, Element 34) is used to compare the X coordinates of the start and end point of the line segment to the horizontal boundaries (LEFTX and RIGHTX) of the clipping area and also to compare the Y coordinates of the start and end point of the line segment to the vertical boundaries (TOPY and BOTTOMY) of the clipping area to produce C0 and C1. An additional boundary clipper (Figure 3, Element 36) relates the same coordinates (X and Y, start and end point) of the line segment to the boundaries (LEFTX, RIGHTX, TOPY, and BOTTOMY) of the larger graphics device coordinate space to produce D0 and D1 (Col. 7, Line 67 – Col. 8, Line 24). In essence, C0 and C1 relate the endpoints of a line segment to the smaller clipping area, while D0 and D1 relate the endpoints of a line segment to the larger graphic device coordinate space (Col. 5, Lines 41-46). Four conditions are then tested (Col. 5-6, Logical Equations 3-6) and a line segment is either drawn, processed, or rejected based upon the equation results (Col. 6, Table 2). While Hartog relies upon two separate areas or boxes (in addition to the display area) to make logical decisions (draw, reject, or process), the Applicants' claimed invention, upon notice that a trivial reject is not possible from the trivial discard guard band comparison, relies upon only the trivial accept guard band (comprised of both the horizontal and vertical accept clip guard bands) to make a trivial accept decision (Page 10, Line 25-Page 11, Line 6).

Morse is directed to a graphics system using clip bits to decide acceptance, rejection, and clipping. A rendering unit sets bits in a clip bits register for each vertex of a geometric primitive. Each bit indicates whether the vertex is inside or outside of a clipping boundary with respect to a clipping plane. A frame buffer controller then

performs clip testing on the entire geometric primitive by performing Boolean operations on the clip bits. The frame buffer can trivially accept or trivially reject the primitive based on the clip testing. If the primitive cannot be trivially accepted or rejected, then the frame buffer controller sends an interrupt to the rendering unit where an exception register helps determine if the reason for the interrupt is the need to clip the primitive. The rendering unit then reads the vertices from the frame buffer controller, clips the primitive, and sends the new vertices to the frame buffer controller (See Abstract).

Morse teaches three-dimensional graphics processing via a three-dimensional graphics pipeline and furthermore discloses a method of clipping primitives. However all combinations of Koss, Fowler, Hartog and Morse fail to disclose the Applicants' claimed invention. As stated in response to Claim 1, Koss and Fowler fail to teach the Applicants' claimed invention. Moreover, the teachings of Koss in view of Fowler and further in view of Hartog and Morse would also not yield the claimed invention. Koss teaches a system that compares coordinate values to the dimensions of a display space without discard guard bands as accepted by the Office Action, while Fowler teaches a single guard band for optimized processing in prior art. Hartog discloses a method for pre-clipping a line lying within a clipping rectangular region which is a subset of a region of a display screen. In such a system line primitive 40 (Figure 2, Element 40 of Applicant) would be rejected by equation (3) producing a logical true. When condition (3) is true, the line is rejected and no further processing takes place on the line (Col. 5, Lines 49-57). The Applicants' claimed invention would allow line primitive 40 because of its pixel contribution to the display space. While Morse does teach of a pipeline and a rendering unit able to clip a primitive (prior art acknowledged by Applicants; Page 13, Lines 14-16), the combination of Morse with Hartog, Koss and Fowler again fails to yield the Applicants' claimed invention. Instead, the teachings of Koss and Fowler teach away from those of Hartog and Morse. Claim 9 is furthermore dependant upon allowable Claim 1 and contains further non-obvious patentable material. The Applicants respectfully believe Claim 9 to be allowable.

With regard to Claim 10, the Applicants respectfully restate the relevant remarks from Claim 1 and Claim 9. Specifically, the Applicants assert that neither Hartog or

Morse disclose the Applicants' claimed invention where first a trivial discard guard band decides if the primitive can be discarded, and then where the trivial accept guard band (Claims 9 and 10) decides if the primitive can be trivially accepted. The Office Action equates the Applicants' vertical accept clip guard band to the guard band clipping boundary of Morse (Figure 4, Element 314) and furthermore equates the Applicants' vertical accept clip guard band to the regular clipping boundary of Morse (Figure 4, Element 312). However, the regular clipping boundary (Element 312) of Morse simply marks the boundary of the display screen while the vertical discard clip guard band is a scaled vertical boundary of the display screen as stated above. In no embodiment of Morse does a vertical or horizontal discard clip band exist. The Applicants respectfully believe that Claim 10, also dependent upon allowable Claim 9 and containing further patentable material, is allowable.

Claims 29 and 30 are in reference to the primitive processor able to execute instructions stored in memory corresponding to the functions described in Claims 9 and 10. As Claims 9 and 10 are allowable, Claims 29 and 30 are also believed to be allowable.

Claims 11-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,111,584 ("Murphy"). Murphy is directed to a rendering system with mini-patch retrieval from local texture storage. Murphy teaches a processor in which textures are retrieved from local storage as n by n patches. By retrieving a multi-pixel patch on each memory read, the frequency of memory accesses and page breaks in particular are reduced, resulting in lower memory access time overhead.

In reference to Claim 11, the Office action cites Koss as teaching a clip code generator comparing coordinates for vertices of the clip-space primitive with screen space coordinates scaled by a discard clip guard band to determine discard clip codes for the clip-space primitive. The Applicants respectfully restate the relevant remarks from Claim 1 reaffirming the Office Action's admittance that Koss fails to teach discard clip

guard bands for clipping processing (Page 4 of Office Action). Since the Office Action admits Koss fails to teach this aspect, the claim is allowable.

While Murphy teaches a host processor or geometry engine able to translate each primitive into a set of fragments, for argument's sake, the combination of Koss in view of Murphy would only produce a computer graphics system having high performance primitive clipping preprocessing able to compare coordinate vales of primitive vertices to coordinate values of clip regions not scaled to include a discard clip guard band, clip if necessary, and then translate the clipped primitives into a set of fragments. The Office Action fails to provide both motivation to combine Koss and Murphy and furthermore fails to include a reference that teaches a discard clip guard band. As a result, the Applicants respectfully believe Claim 11 to be allowable.

Applicants respectfully restate the relevant remarks from the response to Claim 11 and believe Claims 12-14, all dependent upon allowable Claim 11, to also believed to be allowable. Specifically, Koss fails to teach a graphics processing circuit comprising a clip code generator able to compare coordinates for vertices of the clip-space primitive with screen space coordinates scaled by a discard clip guard band as stated on page 4 of the Office Action. In addition, all combinations of Koss and Murphy fail to yield the claimed invention and all motivations to combine are invalid.

Claim 15, dependent upon allowable Claim 11, is also believed to be allowable as Koss again fails to teach a graphics processing circuit capable to compare coordinate values in consideration of Frustum clip planes scaled by an accept clip guard band.

Claim 16 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,111,584 (Murphy) and further in view of U.S. Patent No. 6,359,630 (Morse); Claims 17and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,111,584 (Murphy) and further in view of U.S. Patent No. 6,052,129 ("Fowler"); and Claims 18 and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No.

6,111,584 ("Murphy") in view of U.S. Patent No. 6,052,129 ("Fowler") and further in view of U.S. Patent No. 5,012,433 (Callahan).

Claims 16, 17, 18, 19 and 20 correspond to the graphics processing circuit claims of allowable method Claims 10, 3, 4, 5 and 8, respectively. Furthermore, Claims 16-20 are also ultimately dependent upon allowable Claim 11. The Applicants respectfully restate the relevant remarks from Claims 10, 3, 4, 5, 8 and 11 and believe Claims 16-20 to also be allowable.

In general, Claims 11-20 are in reference to the graphics processing circuit able to process the methods described in Claims 1-10. The Office Action has failed to provide any motivation that would allow the prior art references to be combined in such a manner as to yield the Applicants' claimed invention. The only motivation to produce the claimed invention comes from hindsight analysis of the Applicants' specification. As Claims 1-10 are allowable, Claims 11-20 are also believed to be allowable.

Attached here to is a marked up version of the changes made to the Specification and Claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made."

Applicants respectfully submit that the claims are in condition for allowance, and an early Notice of Allowance is earnestly solicited. The Examiner is invited to telephone the below-listed attorney if the Examiner believes that a telephone conference will expedite the prosecution of the application.

July 4, 2002

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 1, please delete the heading "Field of the Invention" and substitute thereof:

[Field of the Invention] FIELD OF THE INVENTION

On page 1, at line 10, please delete the heading "Background of the Invention" and substitute therefor:

[Background of the Invention] BACKGROUND OF THE INVENTION

On page, 3, please delete the heading "Brief Description of the Drawings" and substitute therefor:

[Brief Description of the Drawings] BRIEF DESCRIPTION OF THE DRAWINGS

On page 4, please delete the heading "Detailed Description" and substitute therefor:

[Detailed Description] DETAILED DESCRIPTION OF THE INVENTION

On page 25, please delete the heading "Abstract of the Invention" and substitute therefor the heading:

[Abstract of the Invention] ABSTRACT OF THE DISCLOSURE

On page 10, please delete the paragraph beginning at line 25 and substitute therefor the following paragraph:

If it is determined at step 108 that a trivial discard of the primitive is not possible, the method proceeds to step 112 where a determination as to whether the primitive can be trivially accepted is performed. In order to determine if the primitive can be trivially

accepted, comparison of the X and Y coordinates for the vertices of the primitive with trivial accept clip values may be performed. The resulting trivial accept X and & clip codes differ from the clip codes determined for [these]those coordinates which are used for making a trivial discard determination. The trivial accept X and Y clip values correspond to the minimum and maximum X and Y values for the display space as scaled to include horizontal and vertical accept clip guard bands. These horizontal and vertical accept clip guard bands are preferably greater than the horizontal and vertical discard clip guard bands such that more tolerance is allowed for trivial accept operations. The scaling used to produce the trivial accept guard band is preferably based on the rasterization limitations of the rasterizer in the graphics processing system.